

Amendments to the Drawings:

The enclosed Submission of Formal Drawings includes changes to Figs. 14A-14E, 14H-14P, 15A, 16A, 16B, 16D, 16F, 17P-17CC (now Figs. 17O-17BB), 18B (now Fig. 18B-4), 18C, 18H, 19H, 33D and 64B.

The following is an itemization of the changes:

In Figs. 14A-14E, 14H-14P, 15A, 16A, 16B, 16D and 16F, in a number of instances the reference numeral PW5 has been changed to PW5B, the reference numeral NW5 has been changed to NW5B, the reference numeral PW12 has been changed to PW12B, and the reference numeral NW12 has been changed to NW12B, as shown on the enclosed Annotated Sheets. These changes are clearly supported, for example, at page 36, lines 14-17, of the substitute specification filed February 18, 2004, where it is indicated that the suffix "B" is used to denote an implanted layer of dopant as opposed to a "well" of dopant. In any event, these changes are merely changes in labeling and as such do not constitute new matter.

Figs. 17P-17CC have been renumbered as Figs. 17O-17BB, respectively, to rectify the omission of Fig. 17O from the application as filed.

To make the drawings more legible, Figs. 18A and 18B have each been split into four drawings, designated Figs. 18A-1 to 18A-4 and Figs. 18B-1 to 18B-4, respectively. The subject matter in Figs. 18A-1 to 18A-4 and 18B-1 to 18B-3 is unchanged. In Fig. 18B-4, the reference numeral 354M has been replaced by the numeral 354L. The numeral 354M was an error. There is no such reference numeral in the application as filed.

In Fig. 18C, the reference numeral 364P, which is referred to at page 66, line 4, of the substitute specification, has been added, and the designation of the source-body contact has been corrected from "S/D" to "S/B".

In Fig. 18H, the reference numeral applicable to the well NW5 has been changed from 354R to 354S to eliminate the conflict with the similarly numbered element in Fig.

18G; and the reference numeral applicable to the deep N layer has been changed from 390G to 390H to eliminate the conflict with the similarly numbered element in Fig. 35A.

In Fig. 19H, the reference numeral 387 has been corrected to 320 to correspond to the designation of the DMOS transistor at page 70, line 7, of the specification.

In Fig. 33D, the reference numeral 486 has been deleted. It is not referenced in the specification.

In Fig. 64B, the description of the 5 volt transistor 306 as been corrected to "PNP."

All of the foregoing changes are shown in red in the enclosed Annotated Marked-up Drawings.

Finally, to place the drawings in sequential order, sheets 215-218 (Figs. 17V-17CC) of have been renumbered as sheets 75-78 (renumbered Figs. 17U-17BB), and sheet 219 (Fig. 18H) has been renumbered as sheet 92.

All of the foregoing amendments are incorporated in the Submission of Formal Drawings, enclosed herewith.

Attachment: Annotated Sheets Showing Changes

REMARKS/ARGUMENTS

It is noted that the specification filed in this case is in the form of the substitute specification that was filed on February 18, 2004 in the parent application (No. 10/262,567). That substitute specification was accepted by the Examiner in the parent case.

The amendments to the specification made herein are intended to conform the specification to the amendments in the drawings, described in the preceding section, and to correct several remaining clerical and syntactical errors. Also, the meaning of the term "annular" has been clarified. No new matter has been added.

A complete set of formal drawings is submitted herewith.

Should the Examiner have any questions about any of the amendments made herein, the Examiner is invited to call the undersigned at (408) 982-8200, ext. 1.

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I hereby certify that this paper or fee is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the below date.



Attorney for Applicant(s)

3/4/05
Date of Signature

Respectfully submitted,

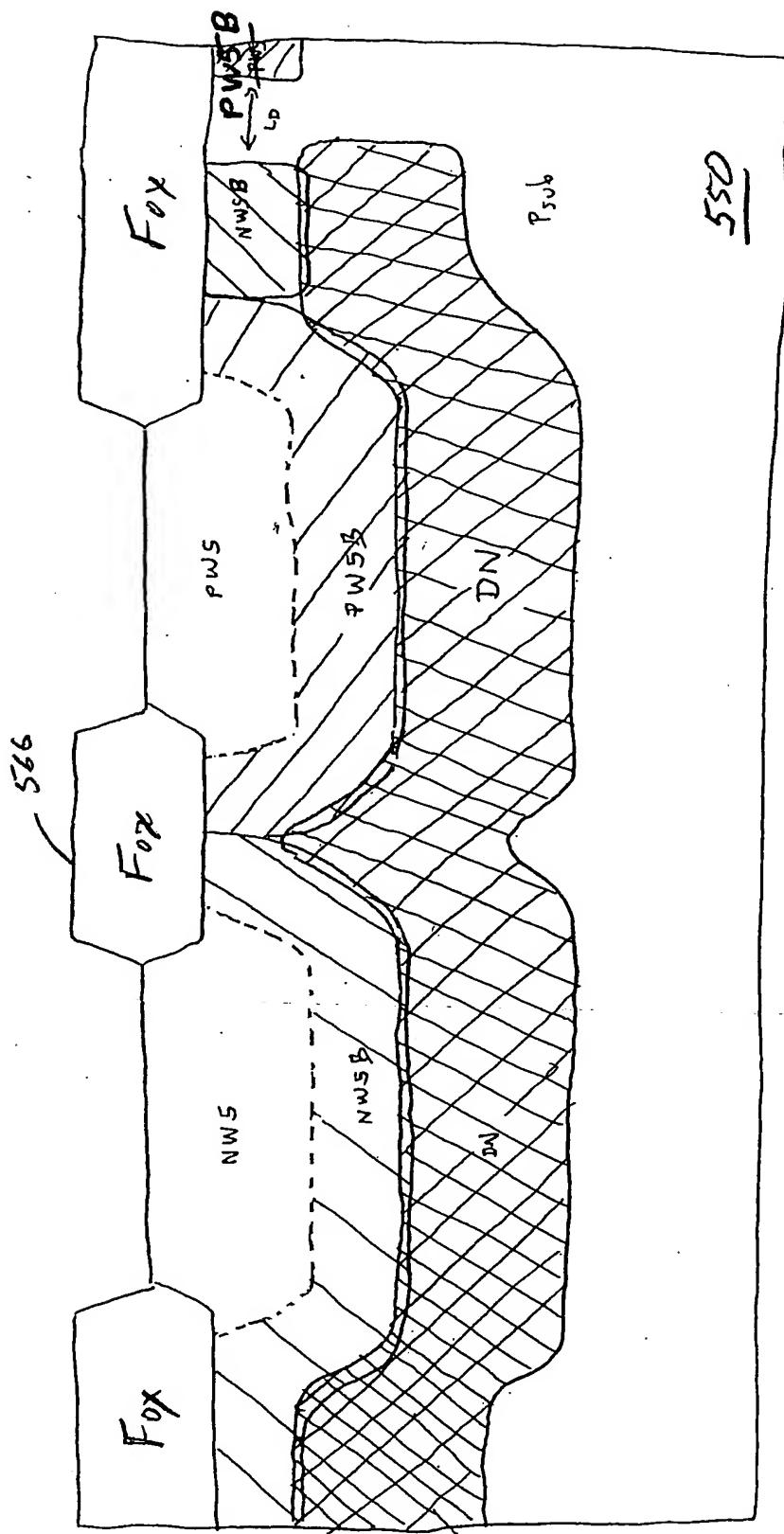


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Reg. No. 25,557



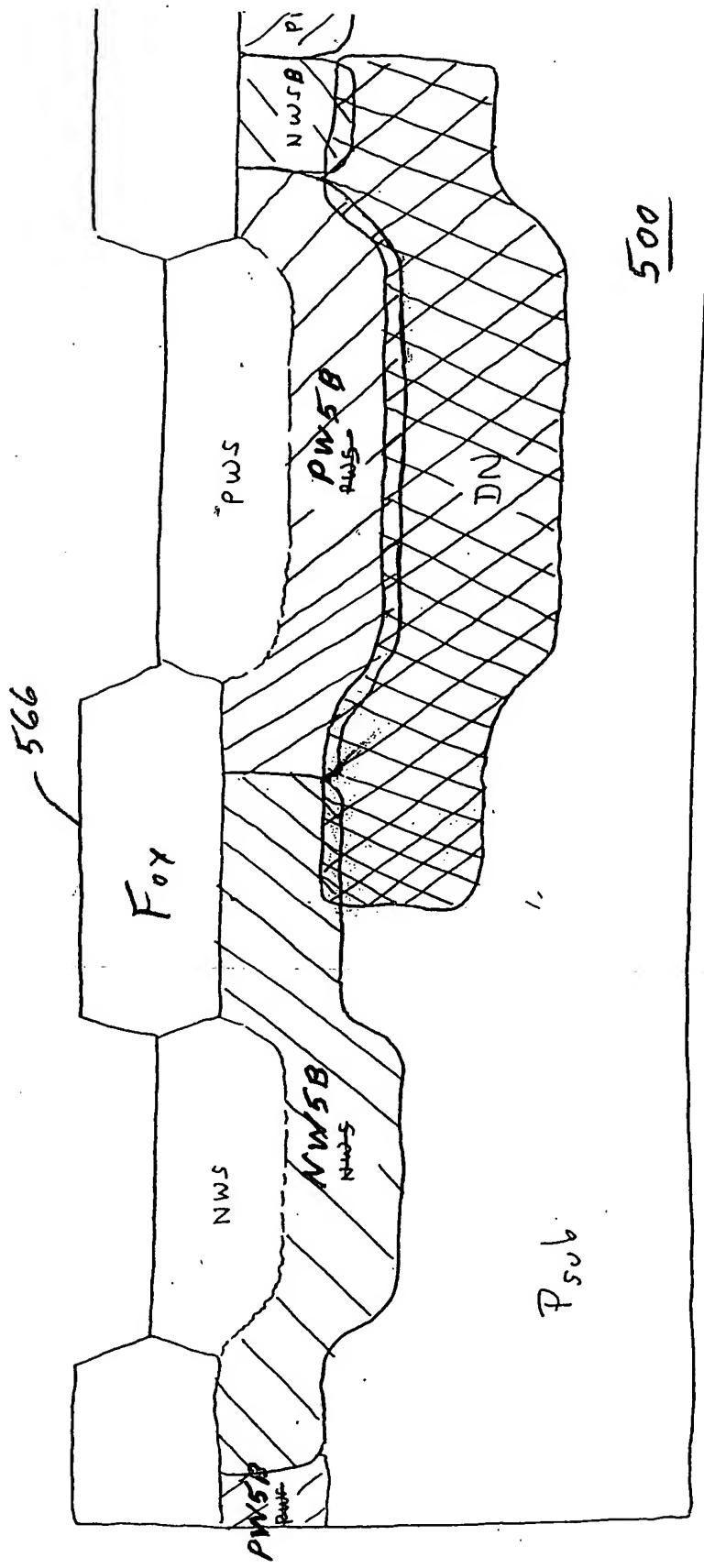
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Fig 14A



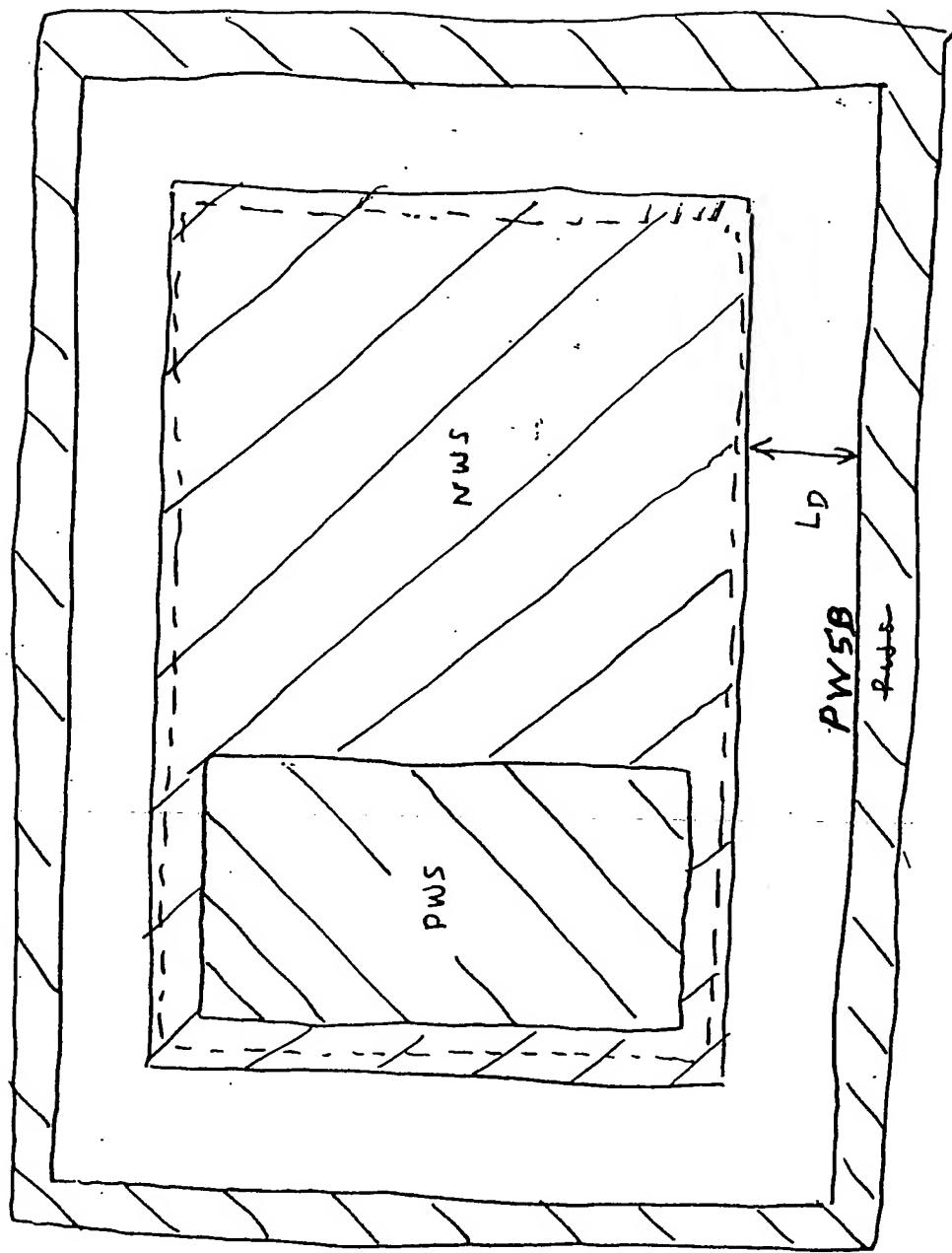
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Fig. 14 B



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FIG. 14 C



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Fig. 14 E

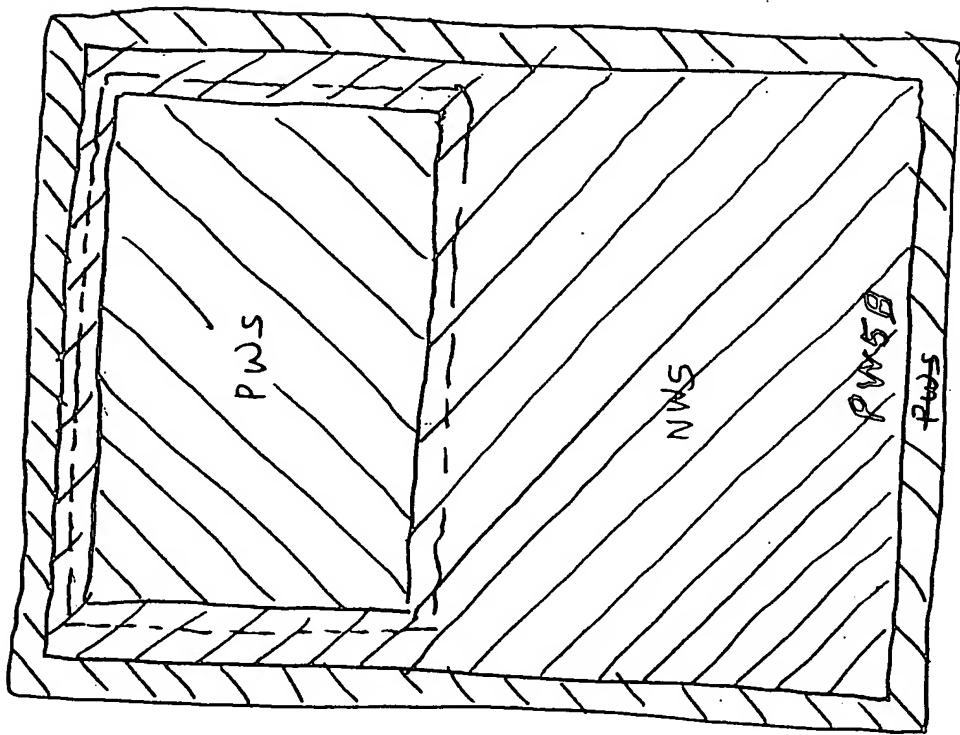
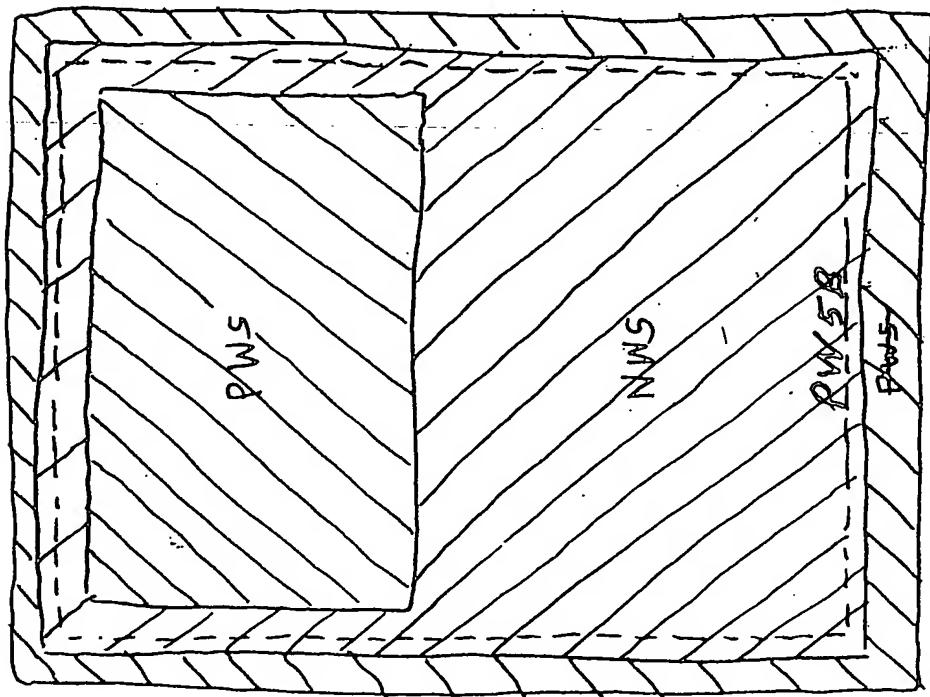


Fig. 14 D



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Fig. 14H

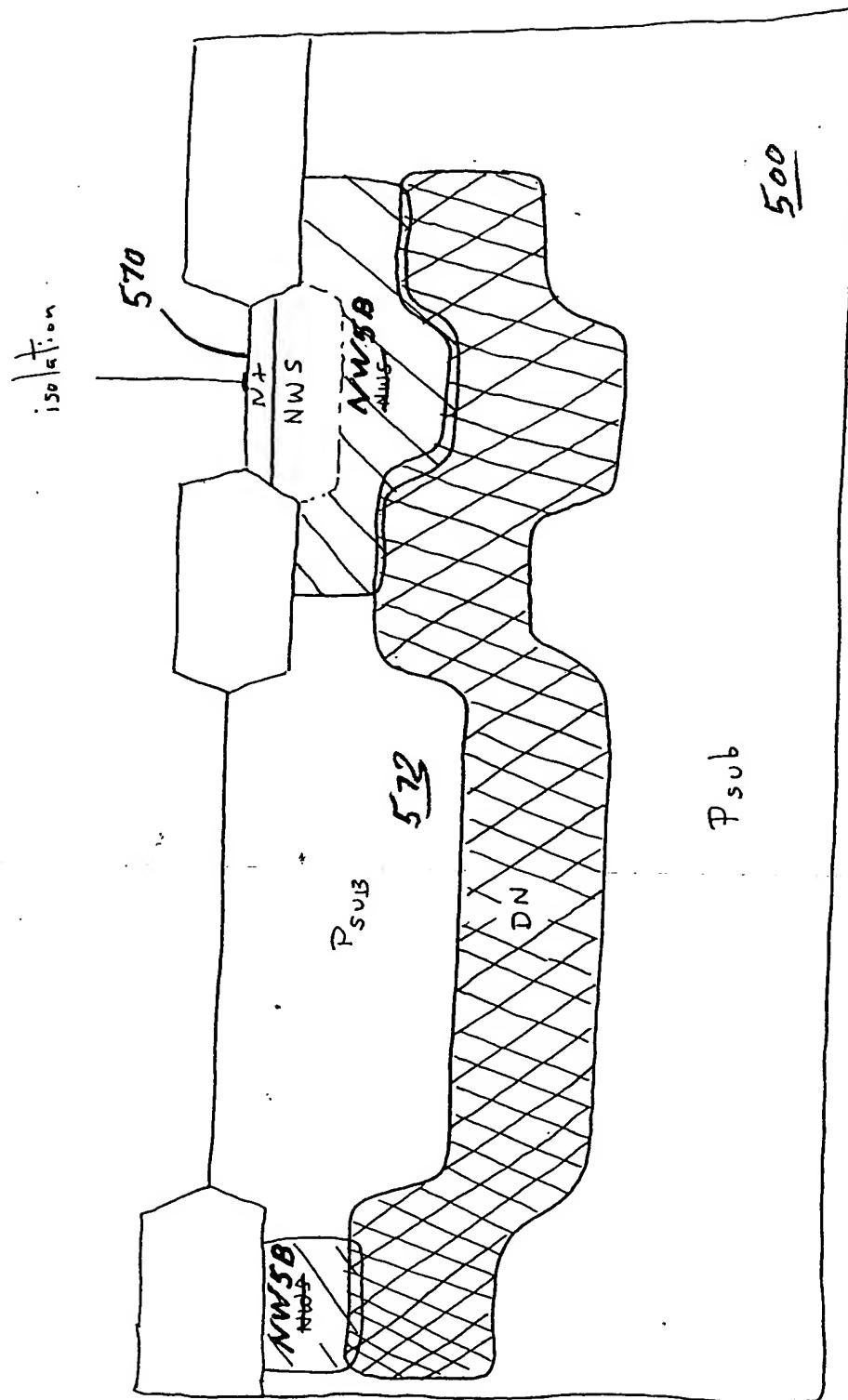


Fig. 14 I.

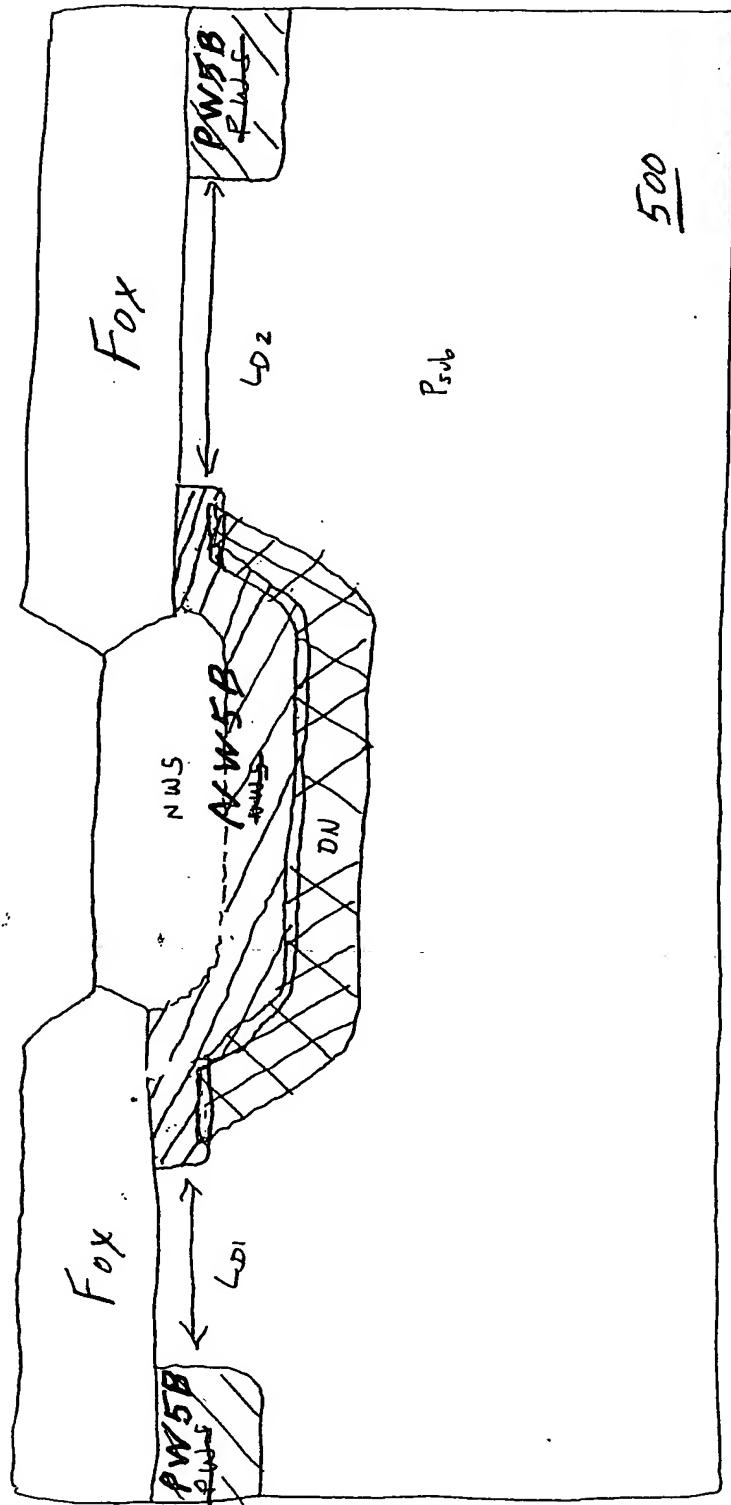


Fig. 14 J

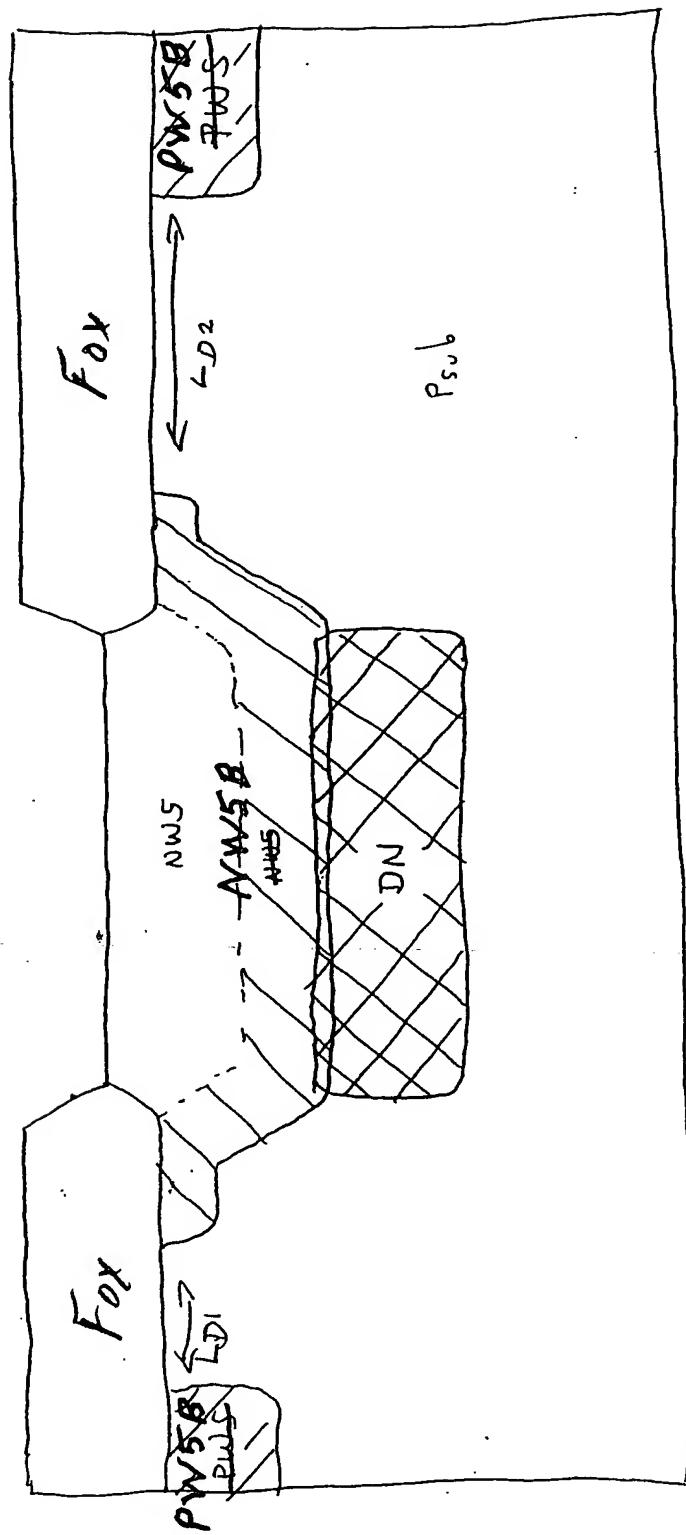


Fig. 14 L

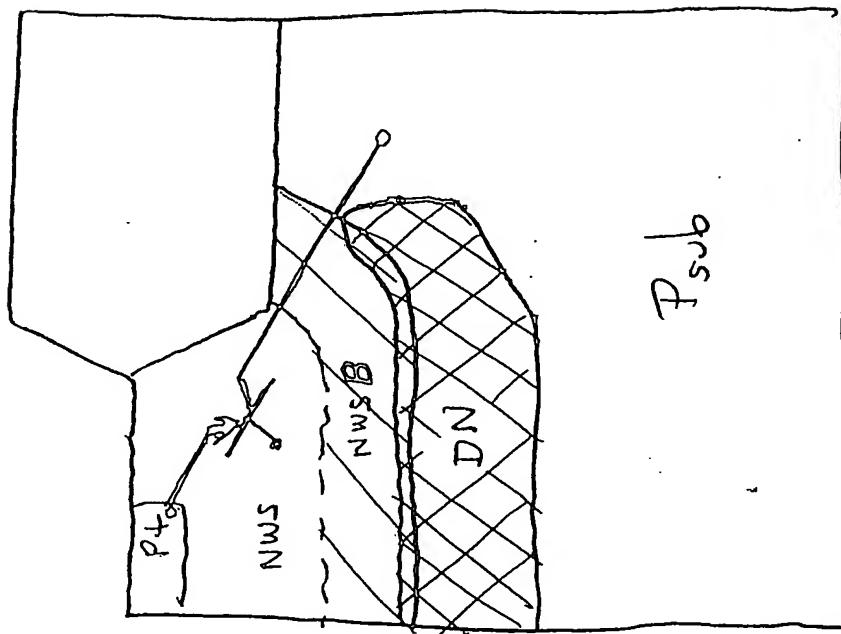
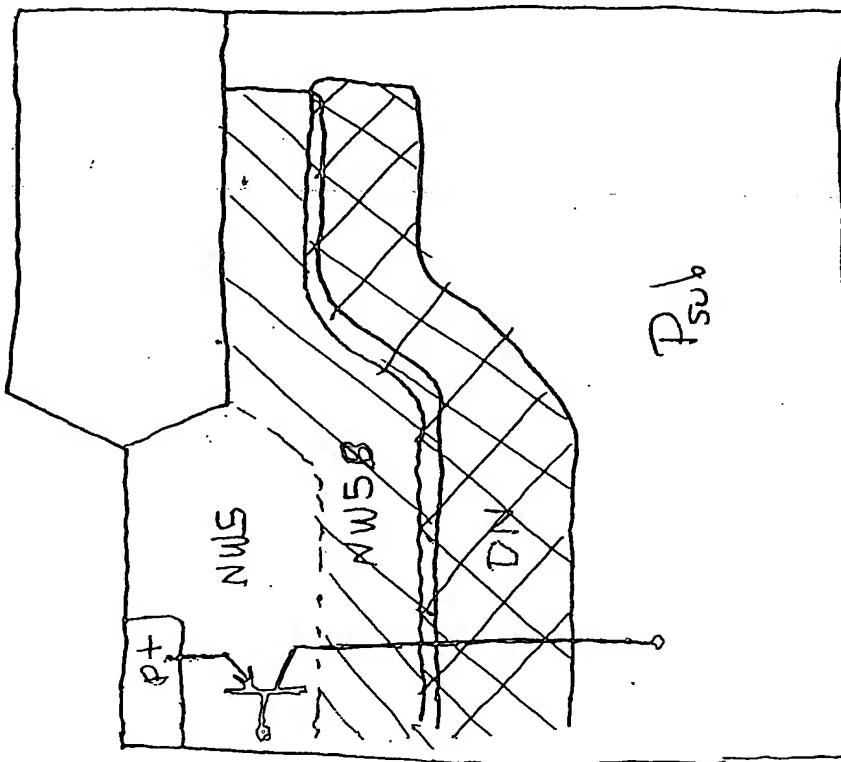


Fig. 14 K

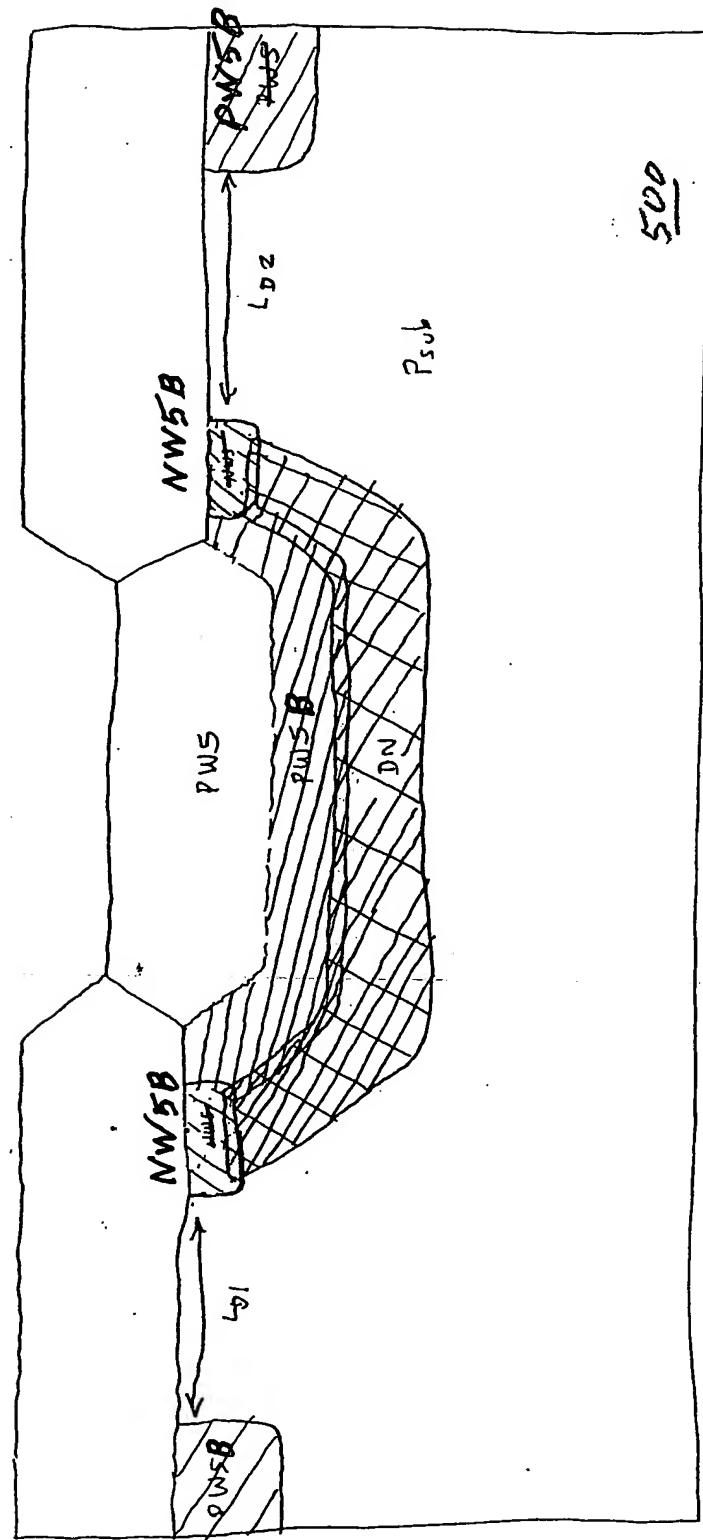


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Fig. 14. A



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Fig. 14P

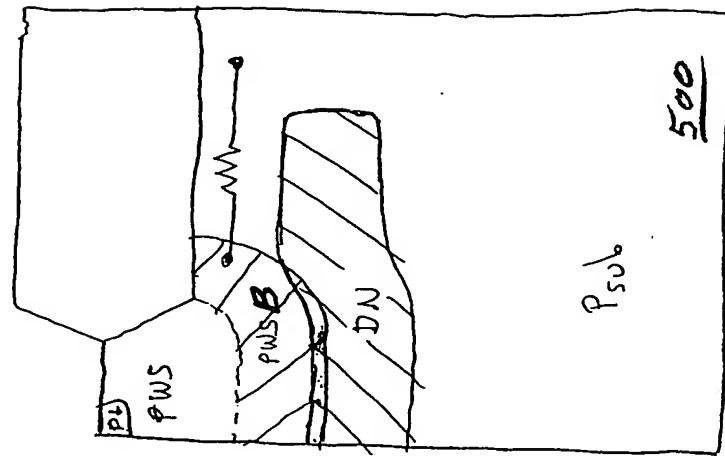


Fig. 14O

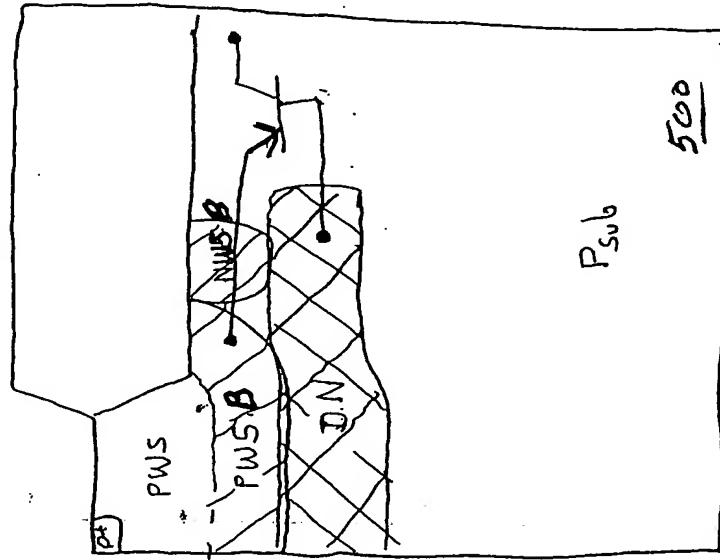


Fig. 14N

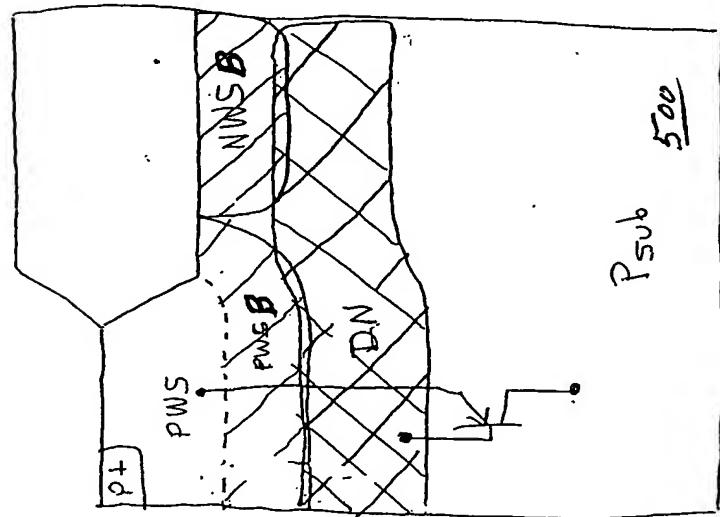
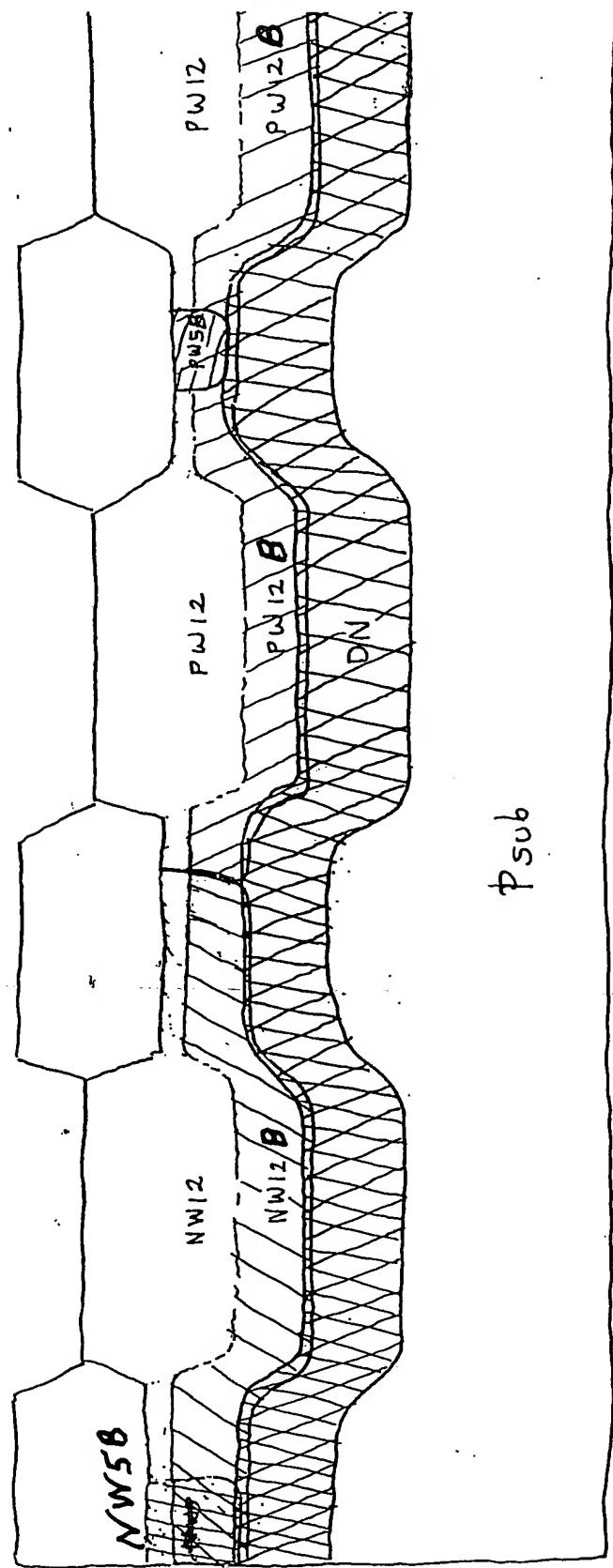


Fig. 15A



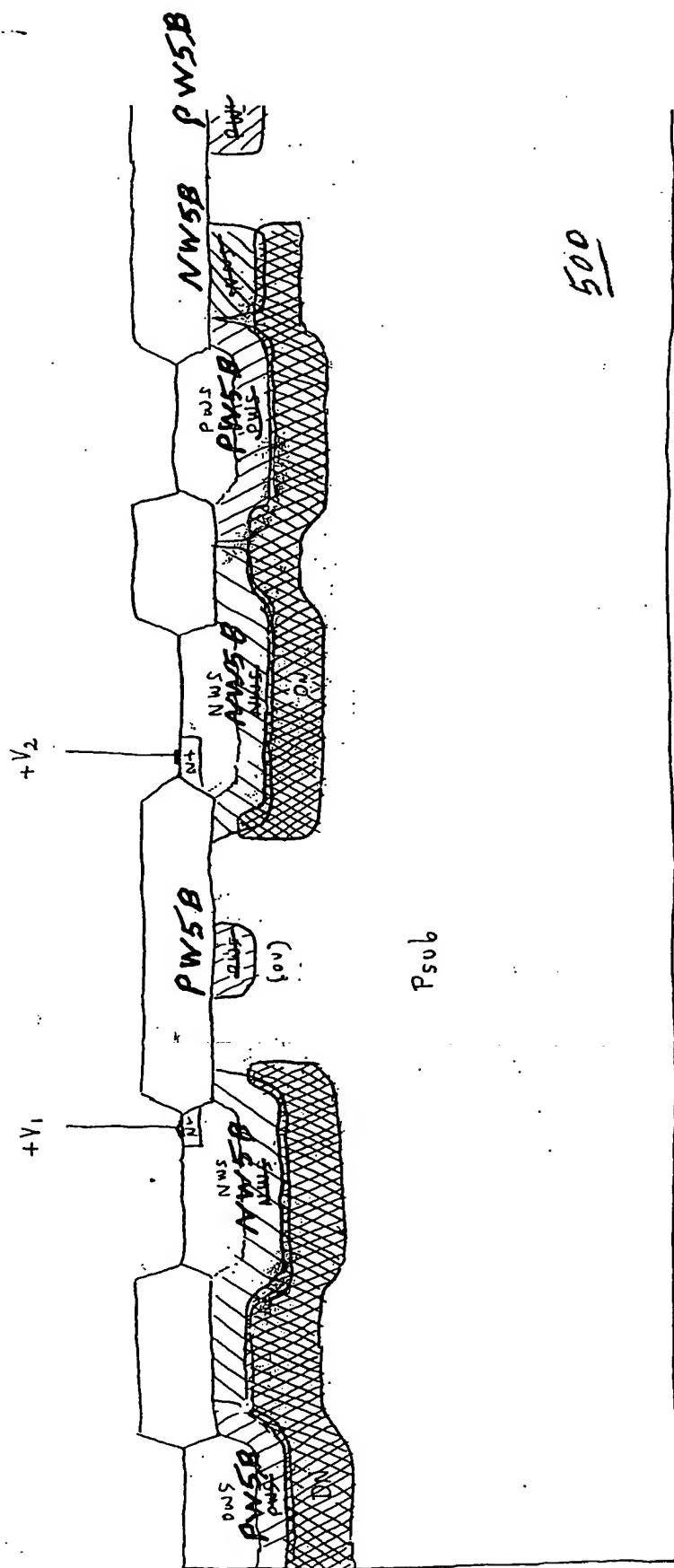
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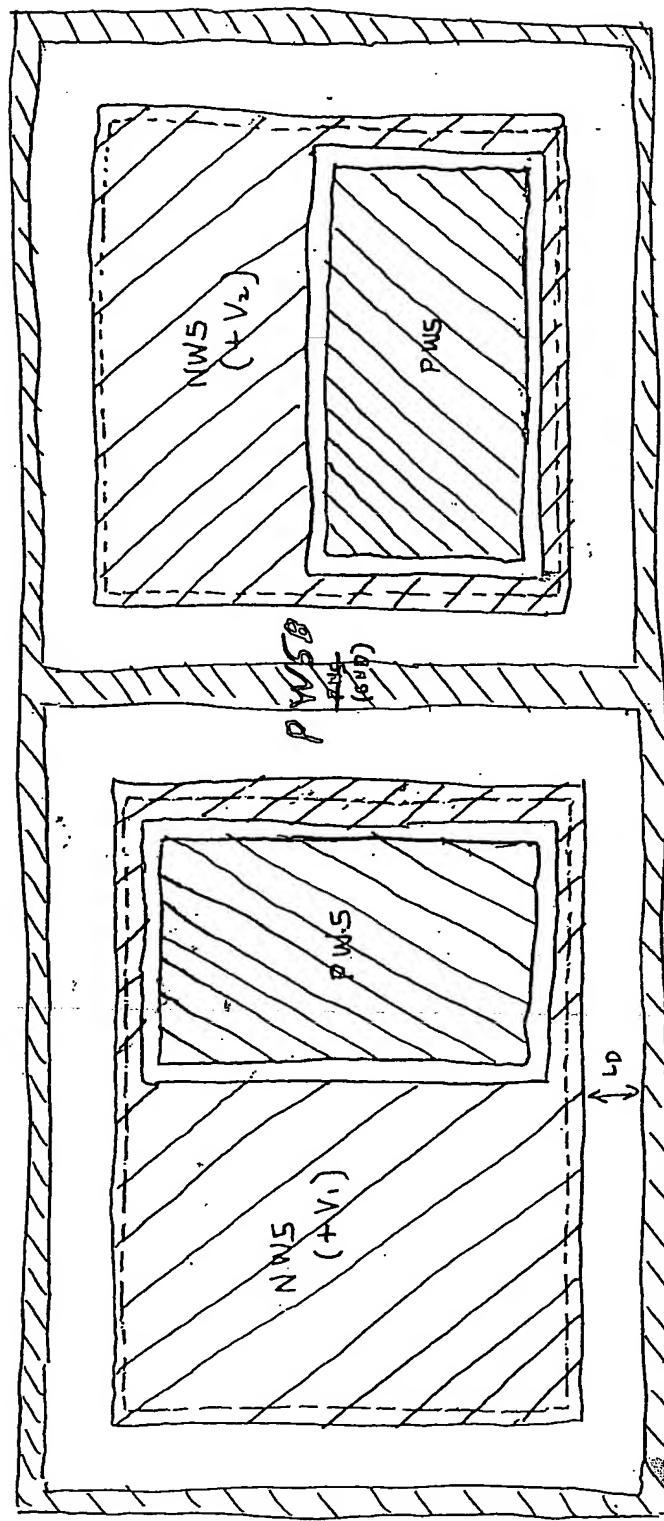
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Fig. 16A



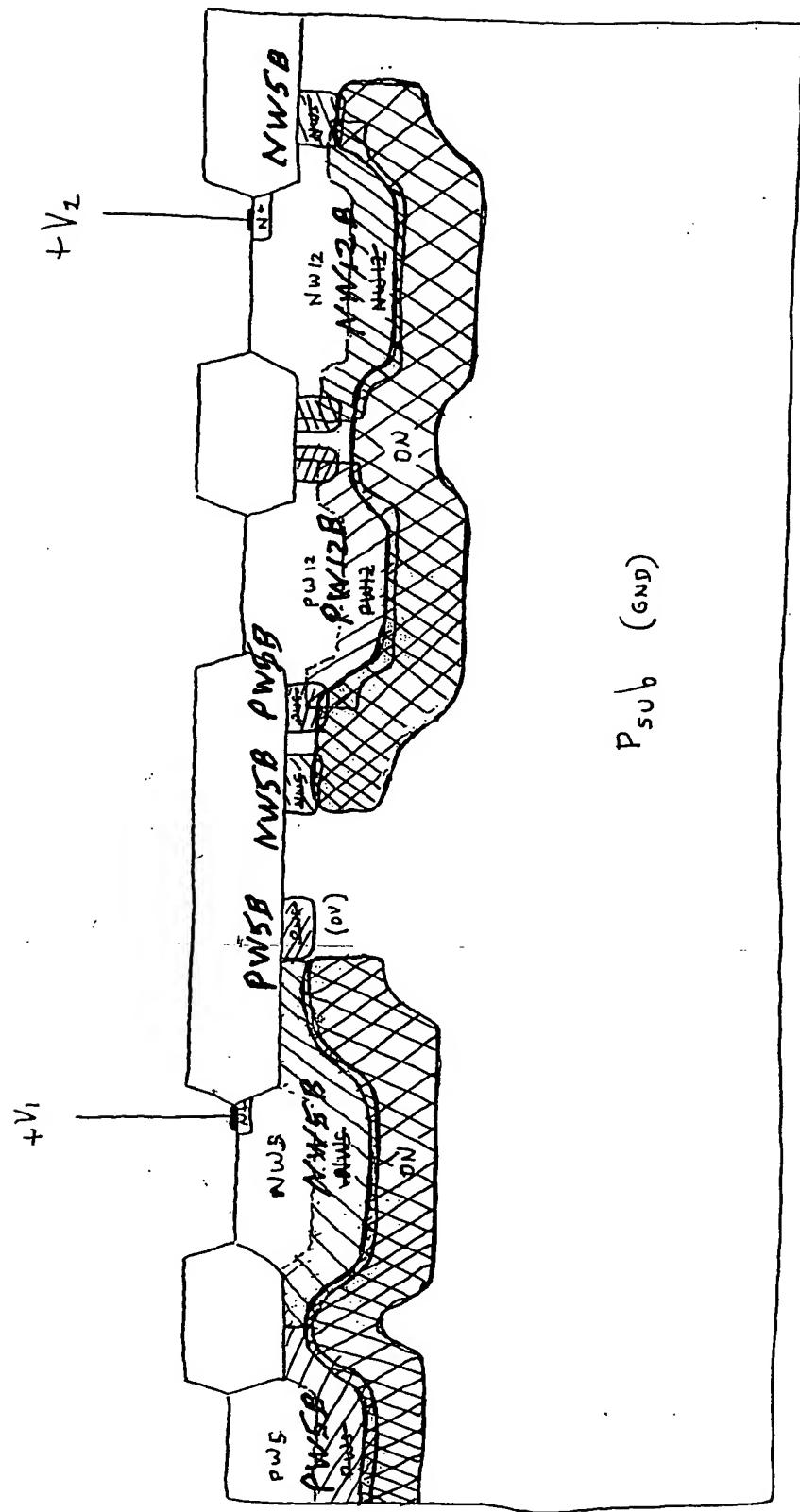
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Fig. 16.3



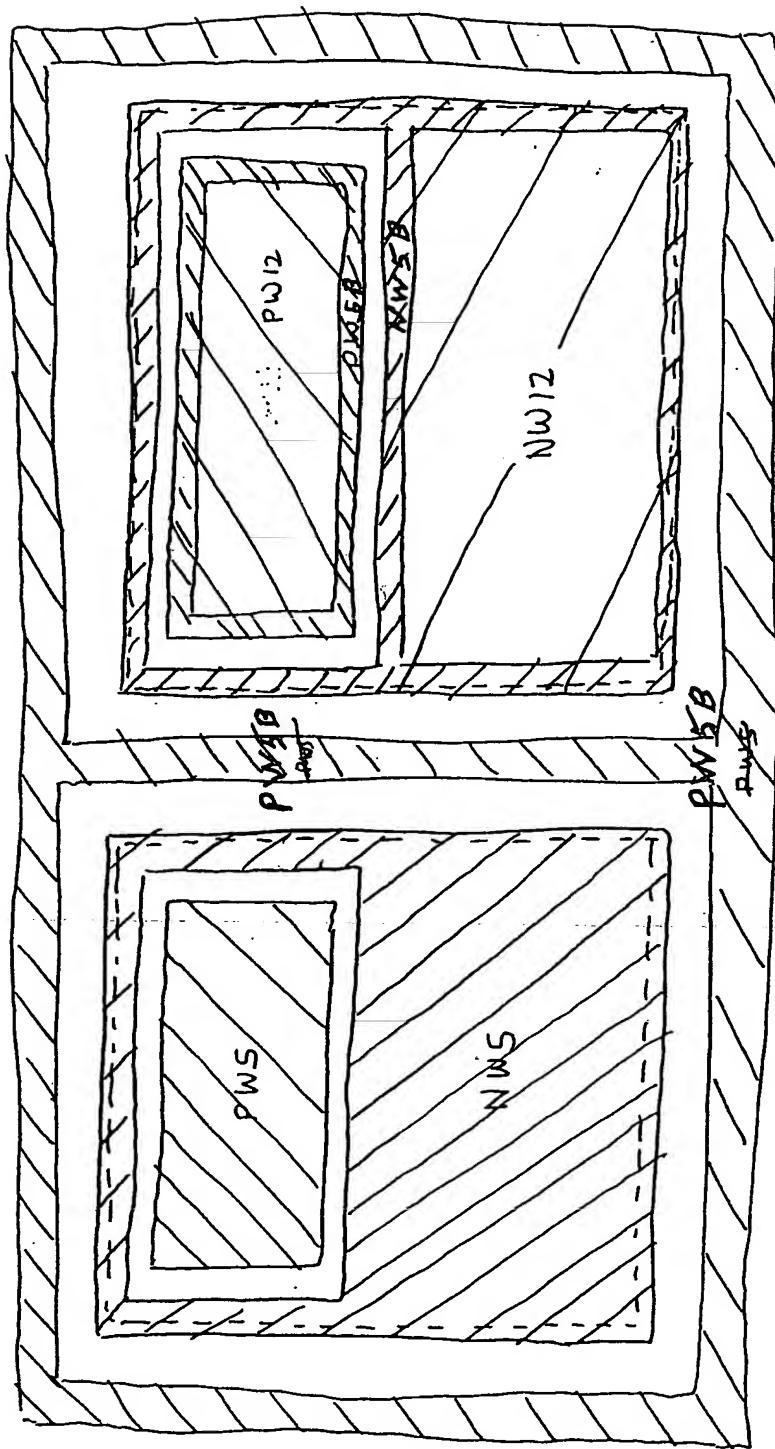
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Fig. 1GD



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Fig. 16F



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Fig. 17Q

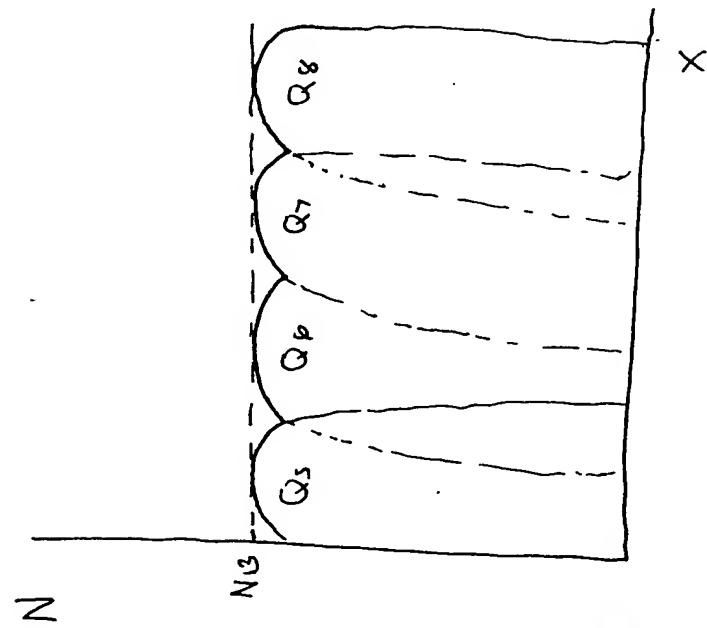
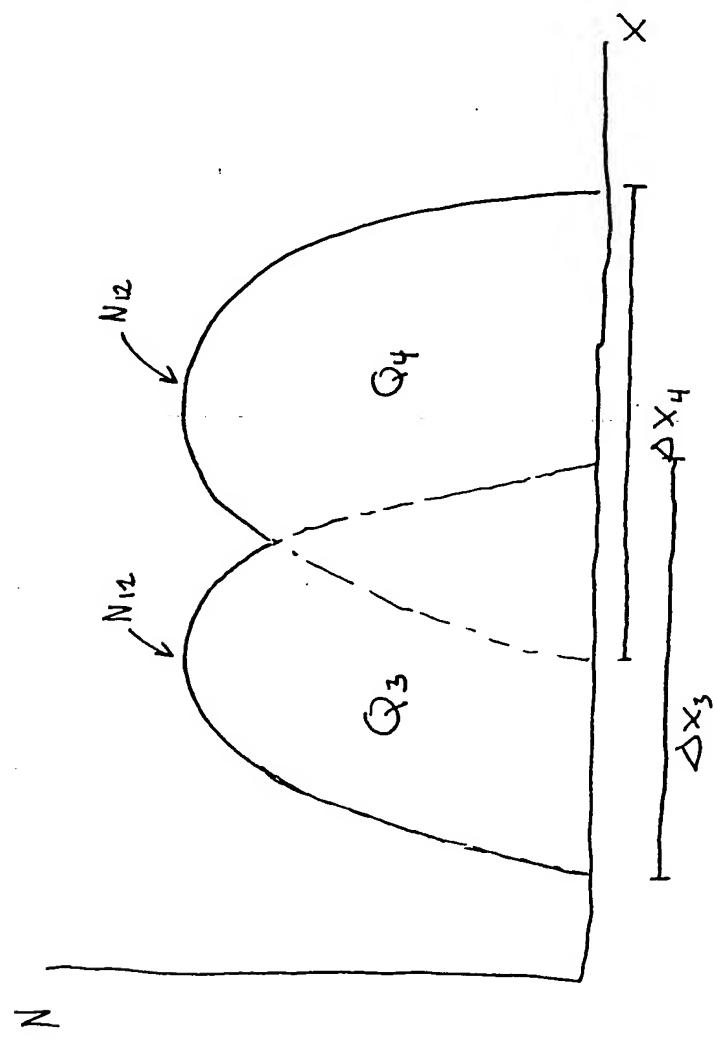


Fig. 17Q



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Fig. 178
R

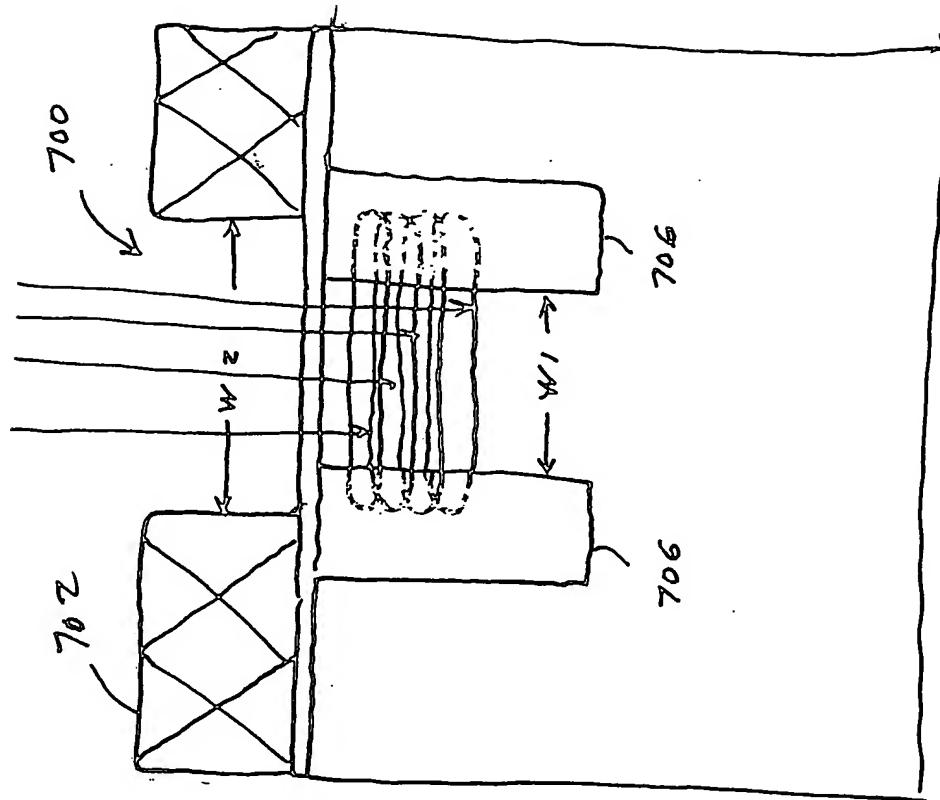
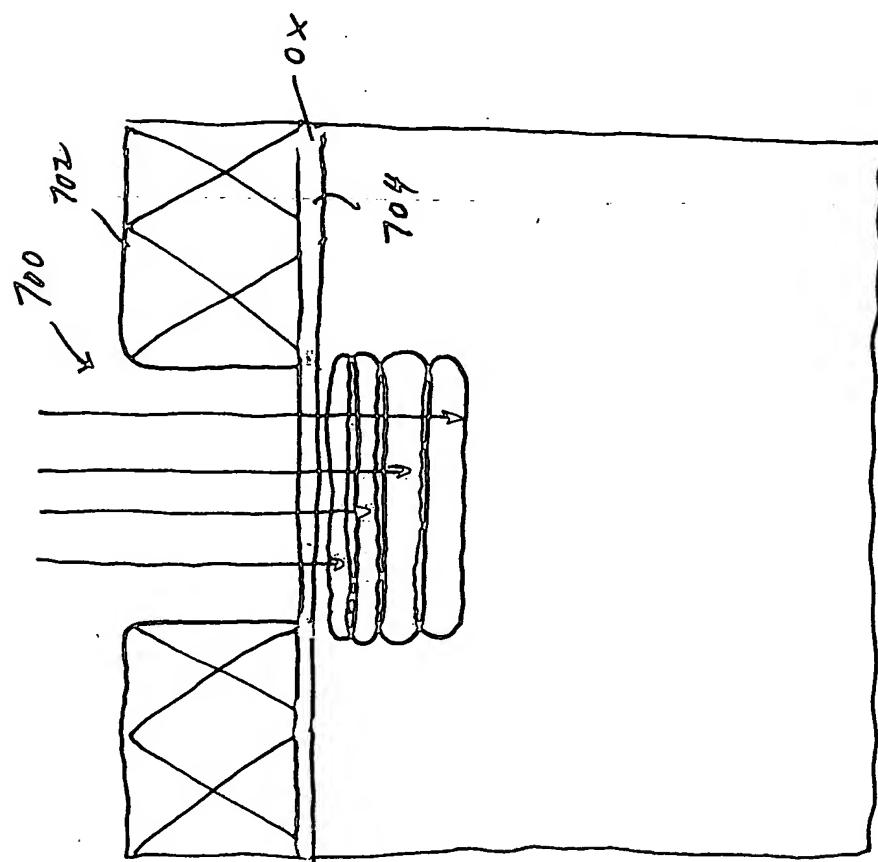


Fig. 178
Q



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Fig. 17A

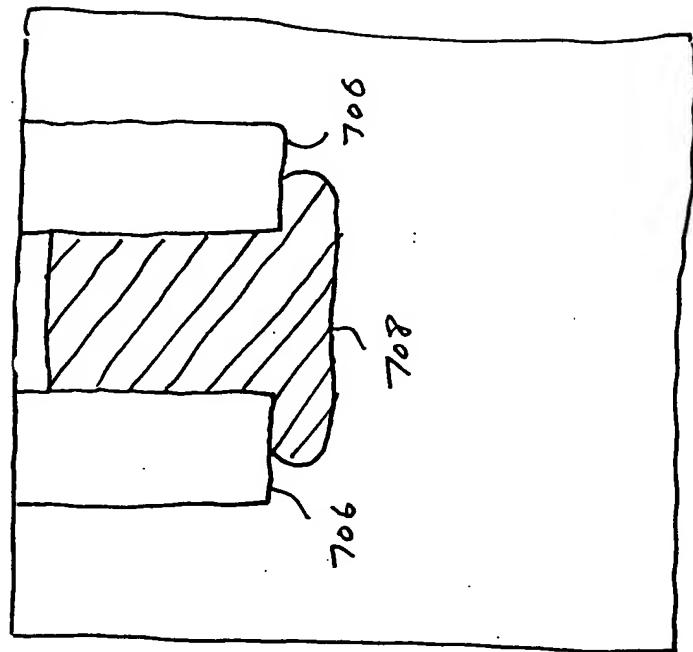
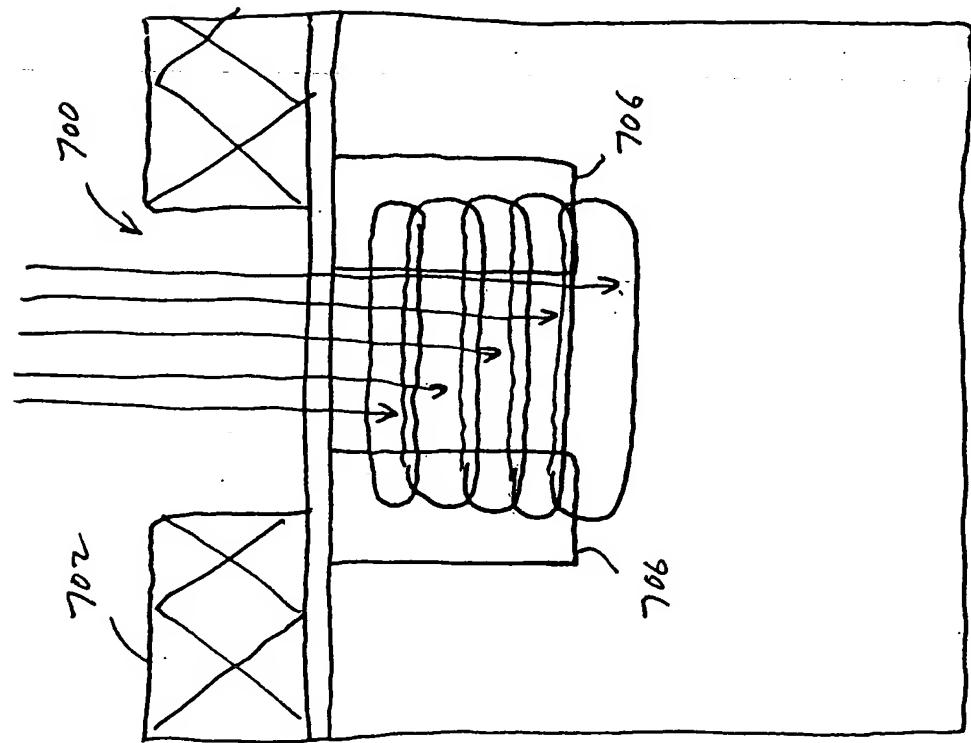


Fig. 17A'



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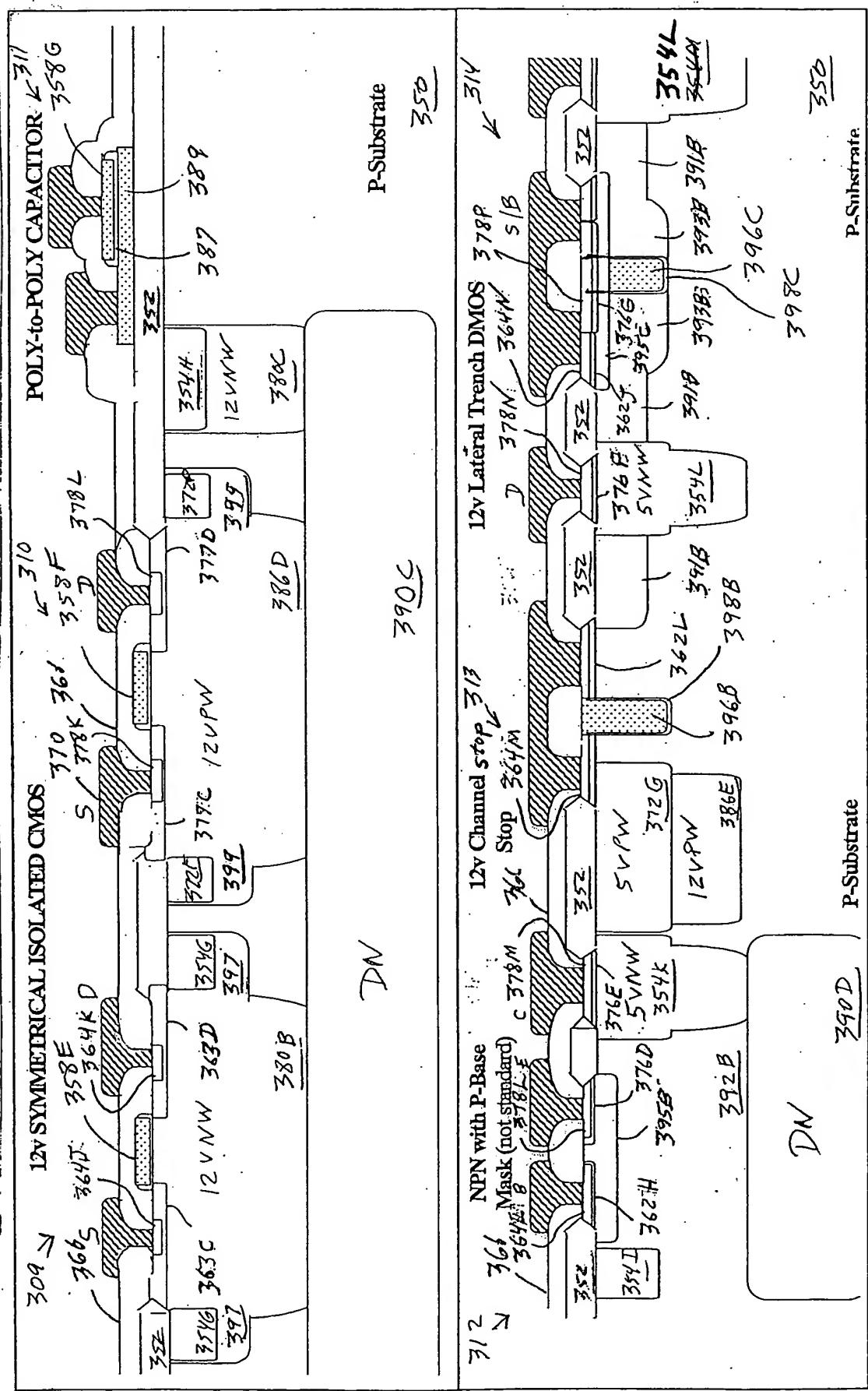


Fig. 18B

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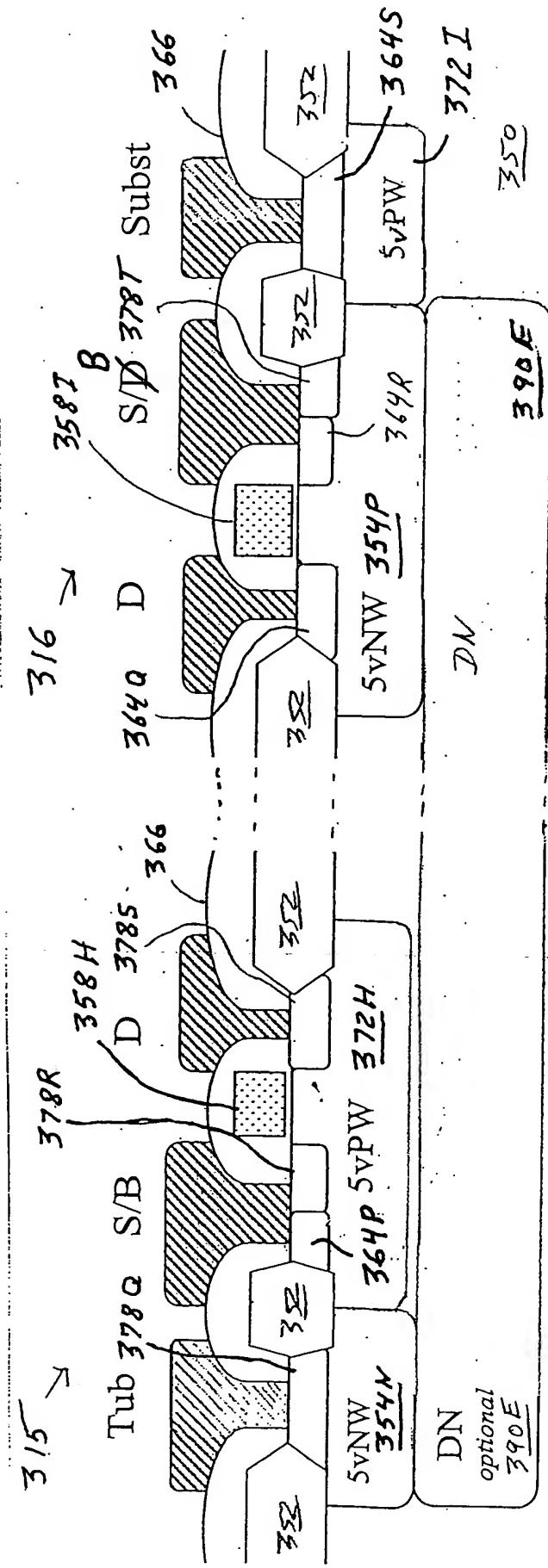
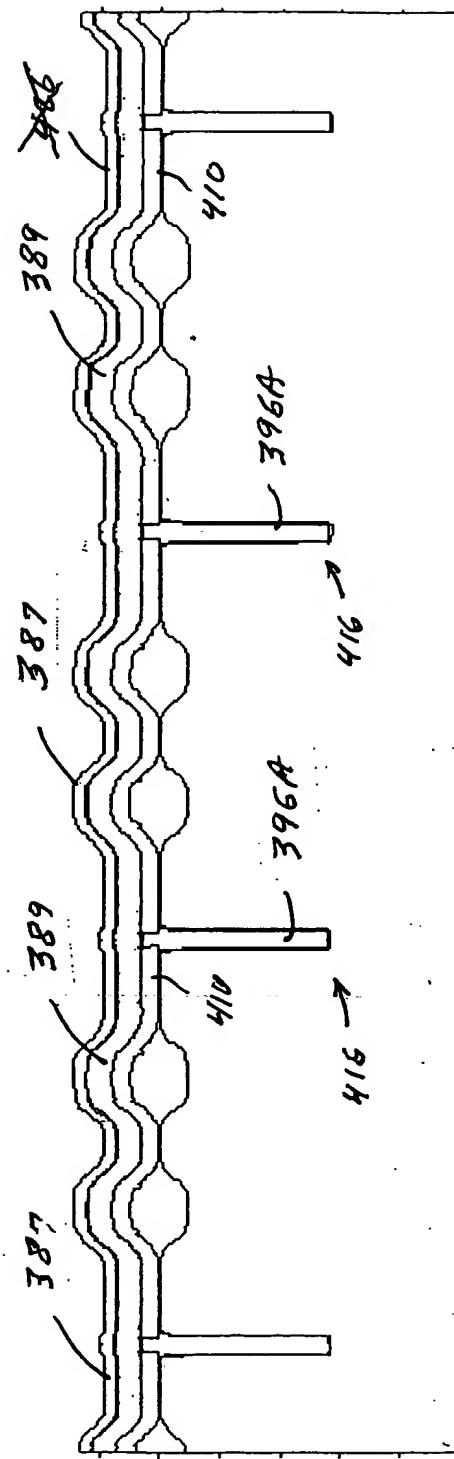


Fig. 18C

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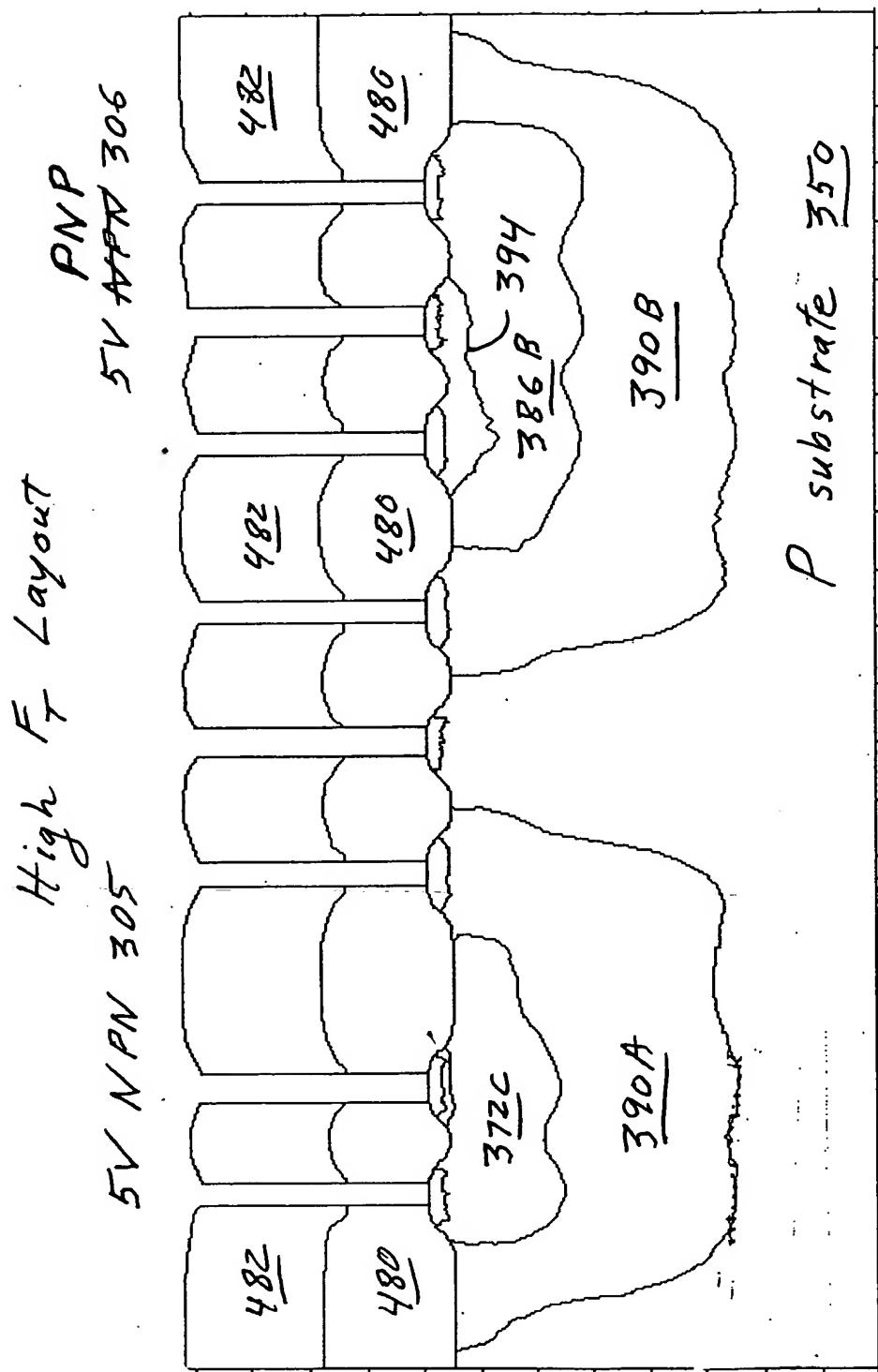
30V Lateral Trench DMOS 308



P substrate 350

Interlayer Dielectric
Fig 33D

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Interlayer Dielectric Deposition and Etch
Fig. 64B

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Fig. 17^U

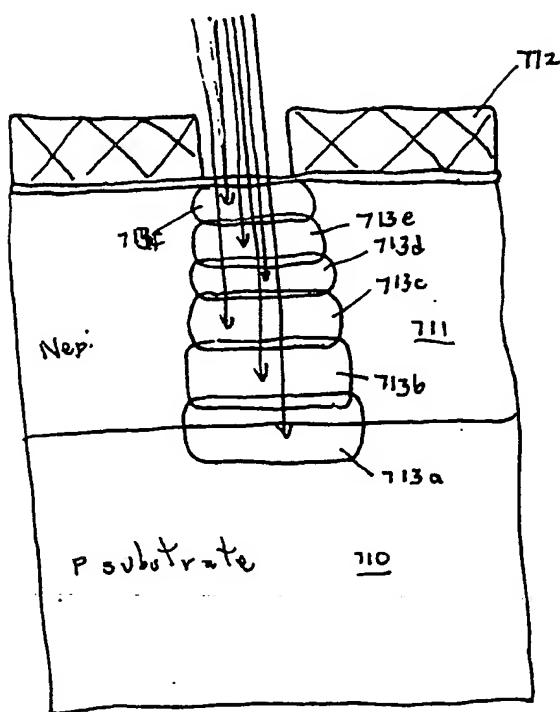
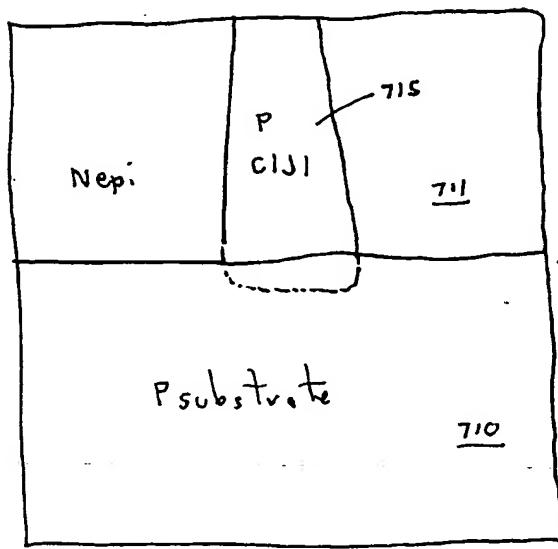


Fig. 17^V



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Fig. 17X ^W

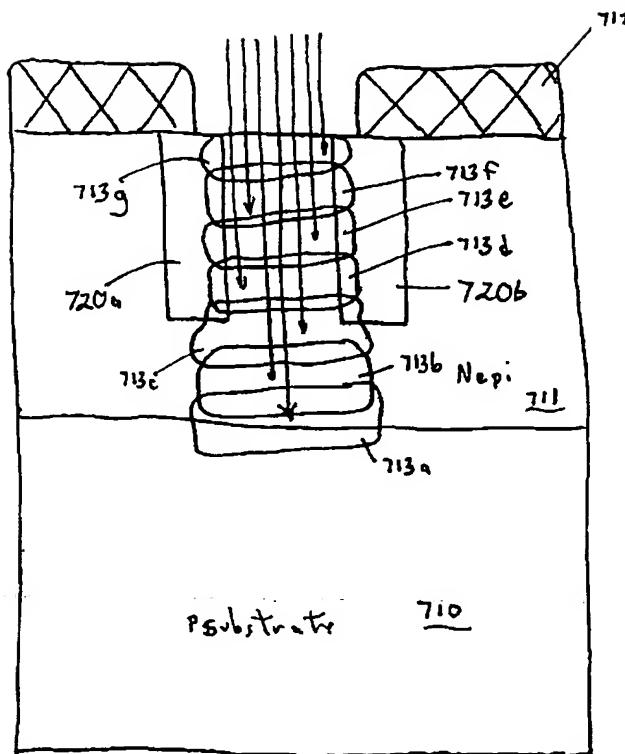
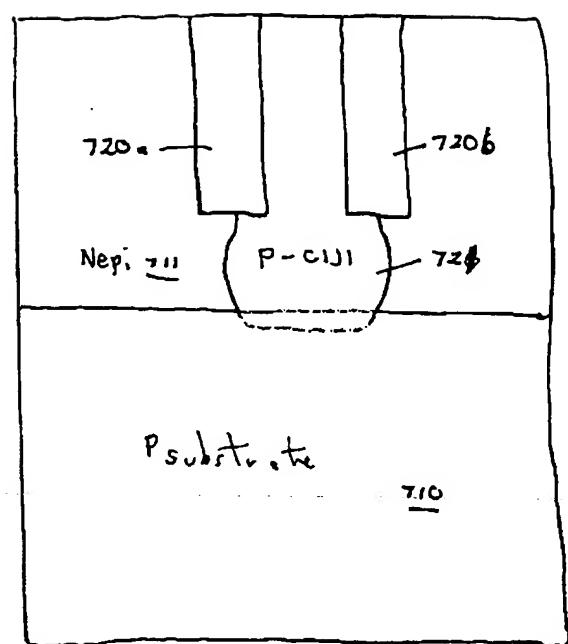


Fig. 17X ^X



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Fig. 17F

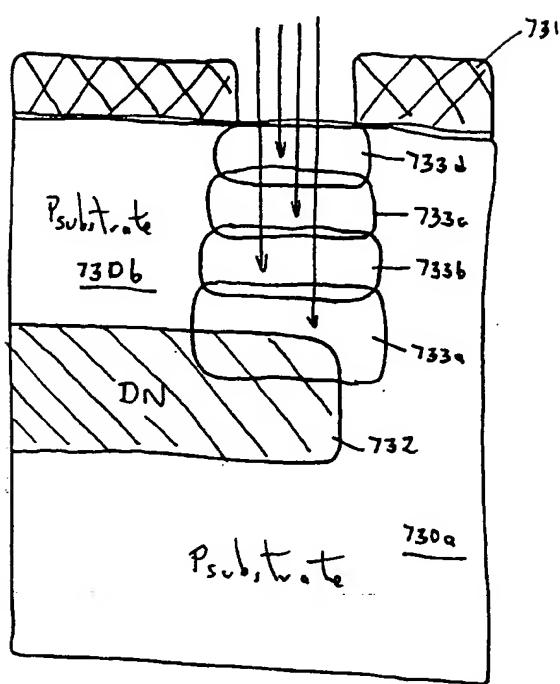
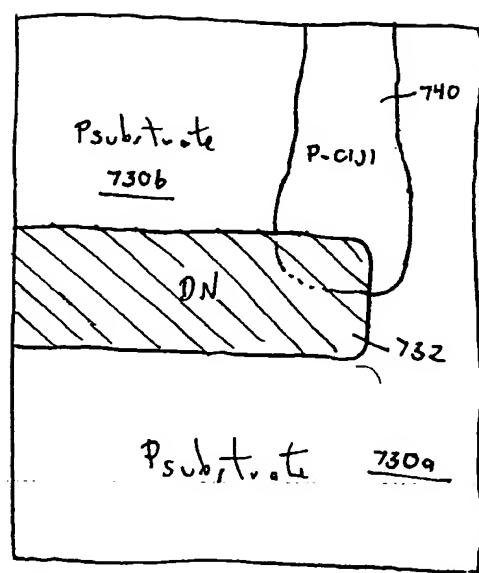


Fig. 17AA



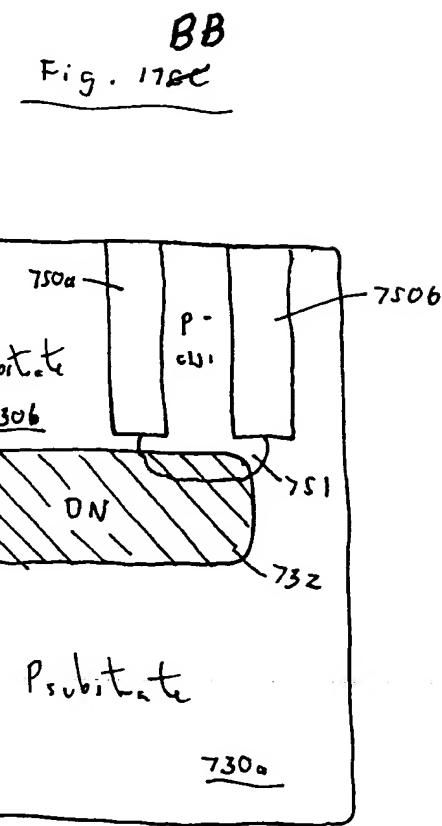
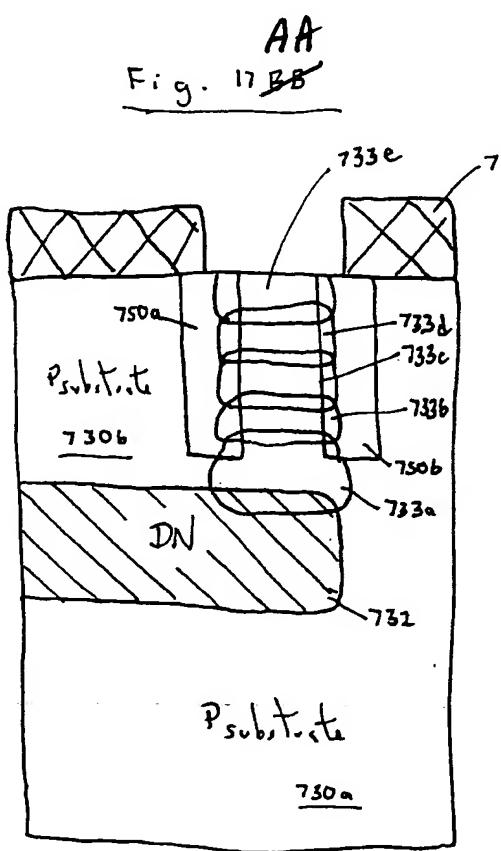
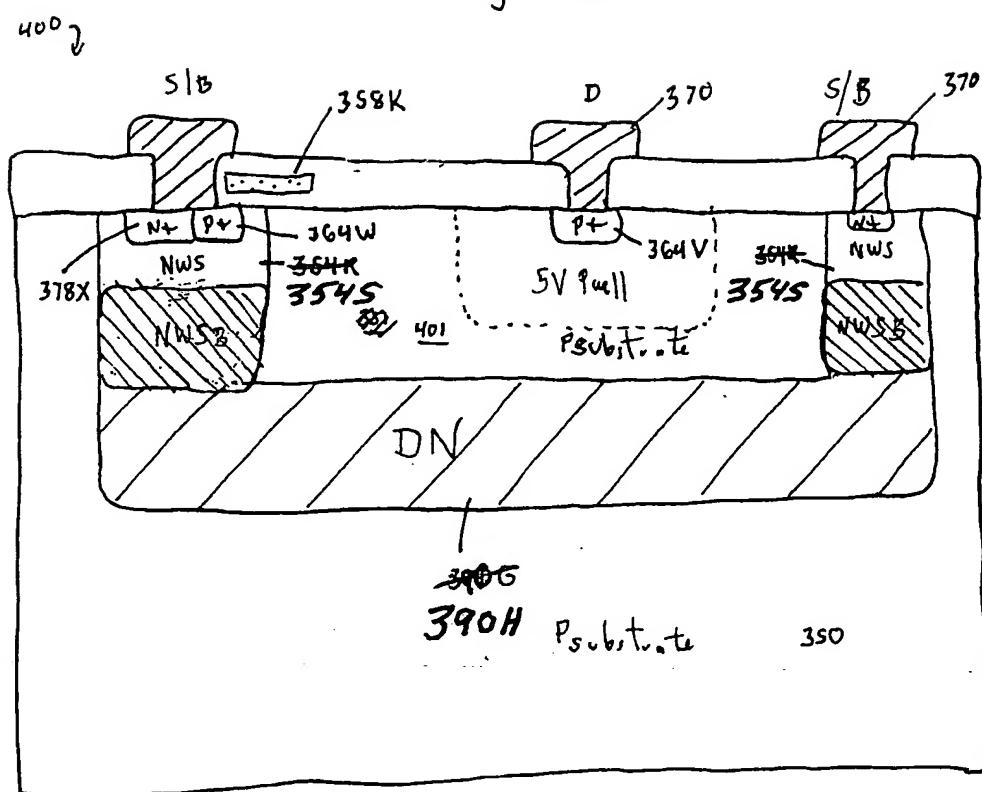


Fig. 18H



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